A 10-Gb/s Two-Dimensional Eye-Opening Monitor in 0.13-μm Standard CMOS

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***Abstract*—An eye-opening monitor (EOM) architecture that can capture a two-dimensional (2-D) map of the eye diagram of a high-speed data signal has been developed. Two single-quadrant phase rotators and one digital-to-analog converter (DAC) are used to generate rectangular masks with variable sizes and aspect ratios. Each mask is overlapped with the received eye diagram and the number of signal transitions inside the mask is recorded as error. The combination of rectangular masks with the same error creates error contours that overall provide a 2-D map of the eye. The authors have implemented a prototype circuit in 0.13-μm standard CMOS technology that operates up to 12.5 Gb/s at 1.2-V supply. The EOM maps the input eye to a 2-D error diagram with up to 68-dB mask error dynamic range. The left and right halves of the eyes are monitored separately to capture horizontally asymmetric eyes. The chip consumes 330 mW and operates reliably with supply voltages as low as 1 V at 10 Gb/s. The authors also present a detailed analysis that verifies if the measurements are in good agreement with the expected results.**

***Index Terms*—Bit error rate, CMOS, eye diagram, eye monitor, eye-opening monitor, high speed, mask error rate, signal quality.**

I. Introduction

THE signal quality in various types of high-speed wireline communication systems such as chip-to-chip interconnects, backplane transceivers, and fiber optic transmission is degraded by jitter and the intersymbol interference (ISI) imposed by the channel. A transversal filter can be inserted in the link front-end to compensate for the channel response and improve the quality of the received signal [1], [2]. For example, Wu *et al.* [3], [4] and Reynolds *et al.* [5] have demonstrated significant bit error rate (BER) reduction by using transversal filter equalizers in the high-speed front-end of multimode fiber links. When the channel response is initially unknown or if it may vary over time, an adaptive equalizer is used in which the transversal filter coefficients are adjusted automatically and continuously to track channel response variations. Since the adaptation is an iterative process, a feedback mechanism is required to measure and report the signal quality at the equalizer output. An eye-opening monitor (EOM) is a circuit block that reports a quantitative measure of the quality of the signal eye diagram (eye pattern) and thus can be used as such feedback.

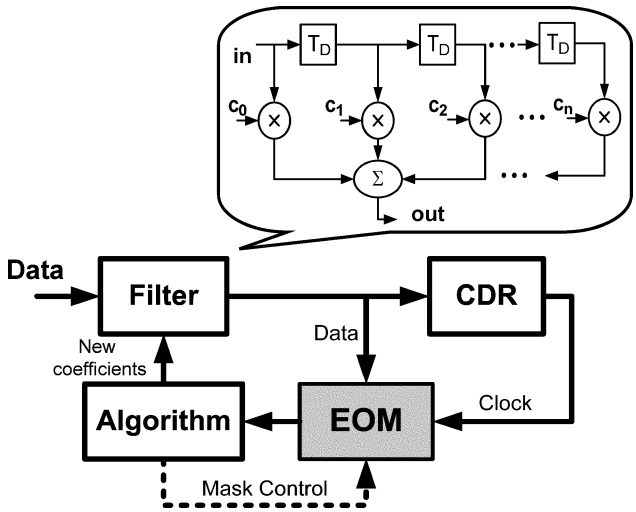

Fig. 1. Adaptive transversal filter equalizer with an EOM.

Fig. 1 shows the block diagram of a transversal filter adaptive equalizer that uses an EOM circuit. The EOM evaluates signal quality by making periodic observations of the filter output and provides information about the filter performance to an optimization algorithm. The algorithm updates all of the filter coefficients accordingly. This architecture is desirable if the transversal filter is implemented using broadband passive delay lines, i.e., LC networks [3]–[5] or active delay elements [6]. At multigigabit per second data rates, the passive or active delay cells become more sensitive to on-chip parasitic components. In contrast to conventional least mean square (LMS) adaptive equalization, when an EOM-based adaptive equalizer is used, the nodes of the delay cells of the filter are not loaded by additional hardware for adaptation circuitry. Therefore, the filter can be designed as a separate module and its response remains intact. The other advantage of the EOM-based architecture is that coefficient optimization is only based on the filter output and is independent of the receiver decision on the symbols. This is especially beneficial in links where training sequences are not used for adaptation and most decisions are erroneous at the startup when BER is high. The EOM can also be utilized as a standalone measurement system to verify the quality of the eye.

The received signal quality in a communication link and the shape of its eye diagram (eye pattern) are strongly correlated [1], [2]. Therefore, eye diagram monitoring has been proposed as a

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technique for extracting information about the received signal [7]–[10] and is used in various applications including adaptive equalizers. George [11] and Hogge [12] both introduced an eye monitor hardware that is used as a pseudo-error detector [7], [13] for rapid estimation of low BER. The estimation is based on evaluating the eye diagrams by comparing them against a fixed rectangular eye-opening mask. Shin *et al.* [14] use an eye monitor to perform a pass/fail test on fiber optic channels. They use two reference levels overlapped with the eye diagram and count the instances that a signal sample is between the reference levels at the sampling time. If the number is more than a given threshold, the channel has failed and another standby fiber channel is selected. Various signal performance monitors have been proposed [15]–[18] to adaptively adjust the decision threshold level of the receiver. For instance, in [16] and [17], the approach is to fit a rectangular mask to the eye and to adaptively adjust its height to keep the number of eye traces occurring inside the mask constant. The traces above and below threshold (representing "1" and "0" bits) are counted separately to capture unbalanced eye shapes. The threshold is set to the center of the rectangular mask. In [17], a separate automatic phase aligner is also included that optimizes the phase of the retiming clock.

Eye-opening monitor circuits have also been utilized as part of adaptive equalizers [19]–[27] mainly to mitigate various dispersion issues in optical fibers. In [22], the eye monitor estimates the vertical eye opening at the sampling point. The receiver includes a path parallel to the main path that embraces a decision circuit with variable decision threshold. The threshold is varied to sweep the eye vertically. The decision of the two paths is compared and an error is recorded if they differ. When the error is integrated over time for various thresholds, the eye vertical opening for a given error rate can be estimated from the separation of the thresholds that resulted in that error rate. Ellermeyer *et al.* suggest a circuit for estimating the horizontal eye opening of the input signal [20], [21]. A rectangular mask with fixed height is overlapped with the input eye. The width of the mask is increased as long as eye traces does not occur inside it and is decreased otherwise. In steady state, the mask width indicates the horizontal eye opening.

In this work, the authors propose an EOM circuit architecture that has the unique feature of mapping both the vertical (amplitude) and the horizontal (temporal) opening of the received eye to a two-dimensional (2-D) error diagram [28]. The error diagram is directly correlated to the eye opening in both dimensions and is essentially the captured image of the signal eye diagram. The output error rate is recorded with a digital counter as opposed to an accumulated or integrated format. This is advantageous when the eye monitor is in a feedback loop with a microcontroller that runs the optimization algorithm because error is recorded in finer resolution and potentially has larger dynamic range. The authors have implemented a prototype of this 2-D EOM circuit in 0.13-μm standard CMOS technology. They have verified its operation up to 12.5 Gb/s. At 10 Gb/s, the error dynamic range is 68 dB. The EOM is not bounded by any architectural limitation at lower data rates. The total power consumption of the circuit is about 330 mW, which is significantly lower than prior work that does not offer concurrent measurement of the horizontal and vertical eye opening.

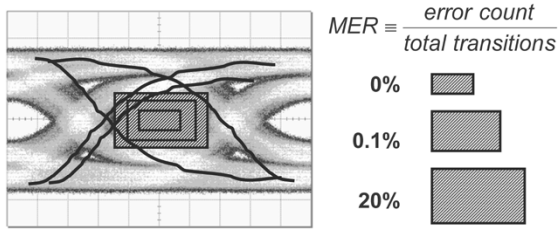

Fig. 2. MER varies for different mask shapes in a given eye diagram.

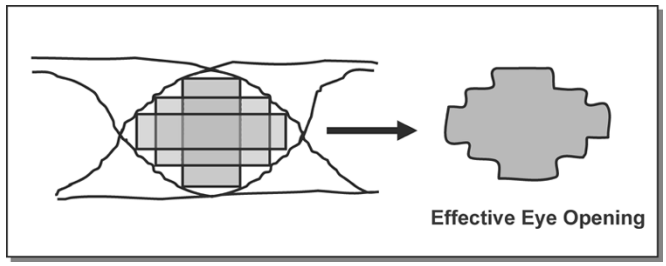

Fig. 3. Effective eye opening formed by combining the mask areas that have the same MER.

The rest of this paper is organized as follows. First, the operation principle of the EOM is discussed in Section II. Then, the designed architecture and its circuit details are presented in Sections III and IV. Finally, the experimental techniques for verifying the operation of the prototype and the measurement results are described in Section V.

II. EOM Principle of Operation

The EOM characterizes the opening of an eye diagram by an eye mask. The eye is overlapped by several rectangular masks with various sizes and aspect ratios. Any eye trace, i.e., data transition, that passes inside a mask is counted as an error. A mask error rate (MER) can be defined as the number of data transitions that fall inside a given mask normalized by the total transitions during the same time period. Fig. 2 illustrates an example where MER is obtained for three different masks in a given eye diagram. Any given mask is associated with an MER that increases as the quality of the monitored eye degrades. The horizontal and vertical opening of an eye can be determined from the mask size for a specific MER. Moreover, different eye diagrams can be quantitatively compared by comparing their associated mask sizes at a given MER. Simply, the eye that can fit a larger mask for the given MER is more desirable. We will discuss the advantages of recording MER, in contrast to the conventional BER, in Section V-F.

A significant feature of a 2-D eye-opening monitor is that it can capture eye diagram shapes with irregular and nonrectangular openings that are common in high-speed links. In such a case, rectangular mask shape might not be the optimum choice for comparing eye openings because nonzero rise and fall times of data transitions constitute a large portion of the bit period and form rounded diamond eye opening. A 2-D EOM can generate rectangular masks of different size in both horizontal and vertical dimensions. For a given eye diagram, a group of masks with different aspect ratio can have the same MER. Fig. 3 demonstrates an example of a typical eye diagram shape overlapped

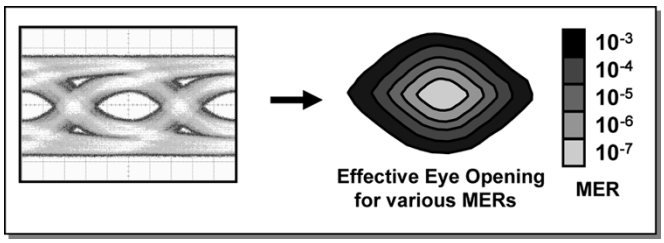

Fig. 4. Combination of effective eye openings is a 2-D error map that is correlated to the shape of the eye diagram.

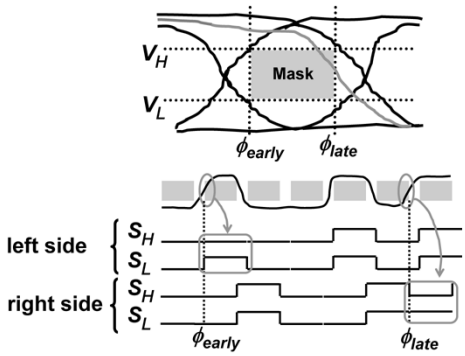

Fig. 5. Operation principle of the EOM for one mask.

with three masks. All the masks result in MER $= 0$. The combined area inside the eye that covers all the masks with the same MER is defined as the effective eye opening at that MER. This effective eye opening is not necessarily rectangular and contains more realistic information about the shape of the eye. The EOM architecture in this design can measure the effective eye opening for different MER values. The aggregate of effective eye openings is a 2-D error map that covers the eye diagram completely and is a representation of the shape of the eye as Fig. 4 illustrates hypothetically.

The MER for a given mask is found from counting the errors, i.e., the number of data transitions that cross either of the two vertical sides of the mask. The operation is demonstrated in Fig. 5. Two reference voltages, V_H and V_L, define the vertical opening of the mask, and two phases of the sampling clock, $\phi_{\rm early}$ and $\phi_{\rm late}$, determine its horizontal opening. Data are continuously compared with V_H and V_L, and these results are sampled at both early and late phases. At each phase, if the sampled values differ, a mask violation has occurred and an error is flagged. The error detection logic is error $= S_H \oplus S_L$, where S_H and S_L are sampled comparison results for either of the phases, i.e., either side of the mask, and the operator is XOR. The timing diagram in Fig. 5 illustrates one violation for each side of the mask. If the errors on the left (from $\phi_{\rm early}$) and right (from $\phi_{\rm late}$) sides of the mask are counted separately, horizontally asymmetrical eye diagrams can be captured effectively. We have added this capability to the architecture by providing two independent error detector blocks for two sides of the mask.

III. EOM Architecture

Fig. 6 shows the proposed architecture of the EOM circuit. Differential input data are compared with differential reference levels in two comparators. The lower comparator reference is generated by swapping V_H and V_L [20], [29]. The reference levels can be adjusted either through an on-chip digital-to-analog converter (DAC) or externally. The DAC sets $V_H = V_{\rm cm} + n\Delta V$ and $V_L = V_{\rm cm} - n\Delta V$, where $V_{\rm cm}$ is the input common mode and $1 \leq n \leq 7$. Every positive edge on next_ref triggers a reference-set shift register that increases n by one. The eighth edge resets n to 1. The step size ΔV is adjustable externally. The comparators' outputs are sampled at both early and late phases by the D-flip-flops (DFFs) that follow the comparators. The sampling clocks are half-rate and thus each DFF block consists of two master–slave DFFs to sample at both rising and falling edges of the clocks. This avoids skipping any data transitions. The samples from early and late phases are processed separately in two independent logic blocks. From discussions in Section II, this allows the EOM to differentiate data transitions that cross the left of the eye mask from those that cross the right side, and enables it to capture asymmetrical eye diagrams. In our prototype implementation, we have combined the early and late errors to only one error_out signal due to test equipment limitations. However, asymmetric eye shapes can still be captured by triggering the early or late sampling phases one at a time. The reference levels are constrained to be symmetric around the input common mode. Thus, vertical asymmetries in the eye cannot be measured.

In each logic block for early or late phases, the errors due to rising and falling edge samples are detected, retimed, and merged. The errors are detected for the edges separately by independent XOR gates. Then, the error signals from the falling sampling edge are resampled at the next rising edge to align the two error signals in time. Then, they are merged by a logic OR function. The merged error signal is divided down by a factor of 16 using current-mode logic (CML). This allows the use of low-power CMOS logic for the dividers in the subsequent stages. Finally, the two error signals from the $\phi_{\rm early}$ and $\phi_{\rm late}$ are retimed by the early sampling phase and are combined. The error output passes through a digital divider with four selectable divide ratios. A larger divide ratio is selected in order to measure cases with high error counts. The chip output, error_out signal, is a toggling output. MER for a fixed mask size can be calculated from the frequency of error_out signal, $f_{\rm error}$, as

$$\text{MER} = \frac{N \times f_{\rm error}}{\text{BR}} \tag{1}$$

where N is the total divide ratio in the chain and BR is the input bit rate. A separate divider chain is used to divide the late sampling clock $\phi_{\rm late}$ by 512. The output is used to monitor clock divider and phase rotator functionality, and is also applied as a trigger signal during the chip test and characterization.

The sampling clocks are generated from an external full-rate clock that is divided by two with an on-chip divider to create half-rate I and Q phases. Two single-quadrant phase rotators interpolate between I and Q to create $\phi_{\rm early}$ and $\phi_{\rm late}$, respectively. Therefore, the output phase of each rotator covers a range of 90° or half of the bit period as can be seen from the timing chart in Fig. 7. Each rotator has 15 thermometer-encoded control lines that set the phase interpolation weights and results in a phase step of 6°. The control line values for each rotator are determined by a phase-set shift register. The trigger signals of

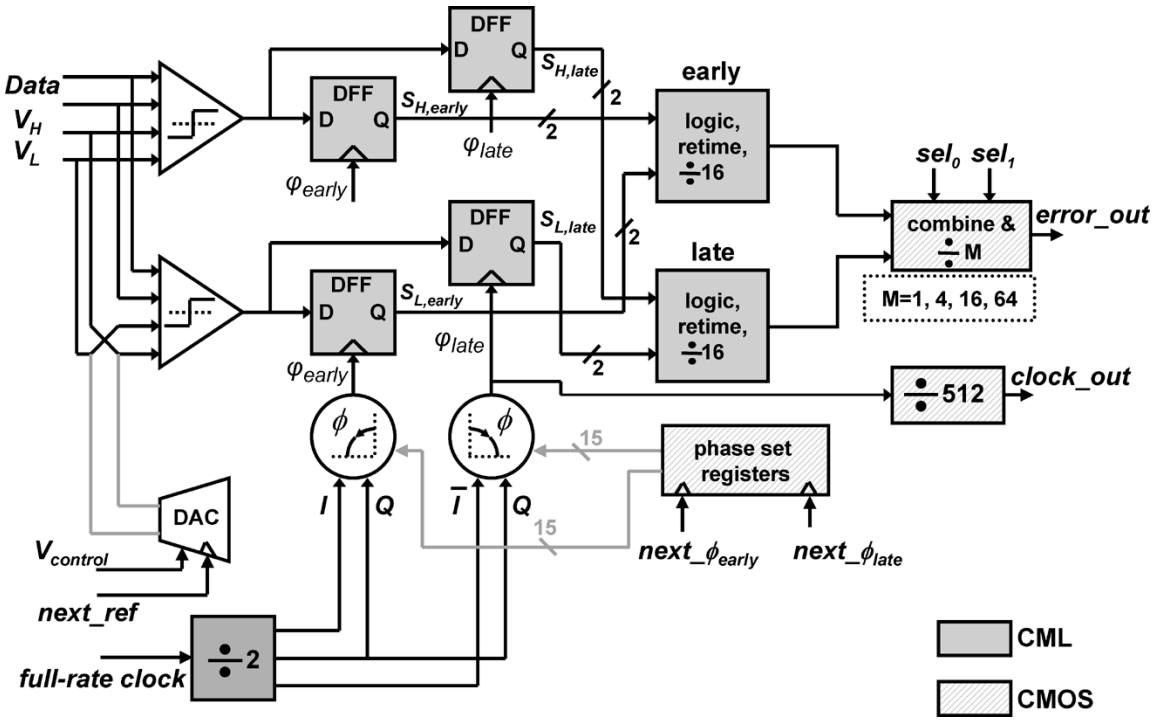

Fig. 6. EOM architecture.

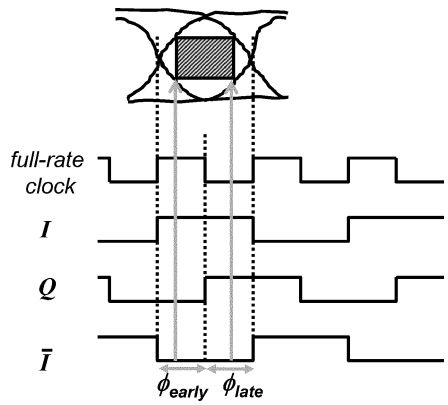

Fig. 7. Generation of $\phi_{\rm early}$ and $\phi_{\rm late}$ by phase interpolation.

the shift registers that increment the control lines for $\phi_{\rm early}$ and $\phi_{\rm late}$ are next_$\phi_{\rm early}$ and next_$\phi_{\rm late}$, respectively. When both control lines are set to zero, $\phi_{\rm early}$ and $\phi_{\rm late}$ have the same phase as Q and overlap in the center of the eye. Every positive edge on next_$\phi_{\rm early}$ moves $\phi_{\rm early}$ one step to the left. Similarly, every positive edge on the next_$\phi_{\rm late}$ moves $\phi_{\rm late}$ one step to the right. The 16th positive edge on either next_$\phi_{\rm early}$ or next_$\phi_{\rm late}$ automatically resets the phase to the center (Q) position.

By separately stepping the next_$\phi_{\rm early}$, next_$\phi_{\rm late}$, and next_ref trigger signals, the architecture provides three degrees of freedom for obtaining several rectangular mask sizes in both horizontal and vertical dimensions. Seven settings for the differential reference voltage DAC and 15 for each phase rotator provide 210 different masks. The number of masks can be increased by applying reference voltages externally with a smaller step size. The MER increases as the mask size expands in either dimension. The EOM can be utilized in two ways. Mask expansion can be stopped at a threshold MER to report the eye opening or all masks can be swept to capture the full error map that represents the effective shape of the eye diagram.

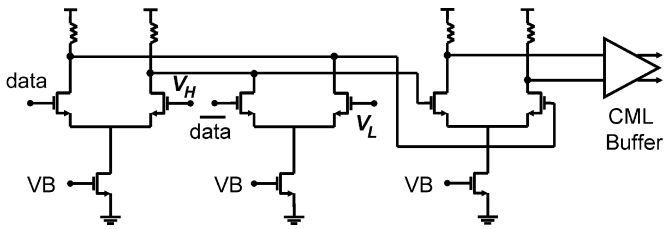

Fig. 8. Differential comparator circuit.

IV. Circuit Implementation

The comparator circuits use a two-stage differential topology followed by a CML buffer, as shown in Fig. 8. The first stage consists of two parallel source-coupled pairs [29]. The overall output of the stage is

$$v_o = g_m R\left[(v_i - V_H) - (\overline{v}_i - V_L)\right] \tag{2}$$

which can be rewritten as

$$v_o = g_m R\left[(v_i - \overline{v}_i) - (V_H - V_L)\right]. \tag{3}$$

The latter is the desired output for a differential comparator with differential reference voltage. The parameters g_m and R in both (2) and (3) are, respectively, the transconductance of one MOS transistor and the load resistor. Since the reference voltages V_H and V_L are stepped such that all the input swing range is covered by the vertical mask opening, each source-coupled pair must tolerate a wide range of common-mode input and thus needs a large common-mode rejection ratio (CMRR). The second stage is also added to enhance the CMRR of the comparator and to increase

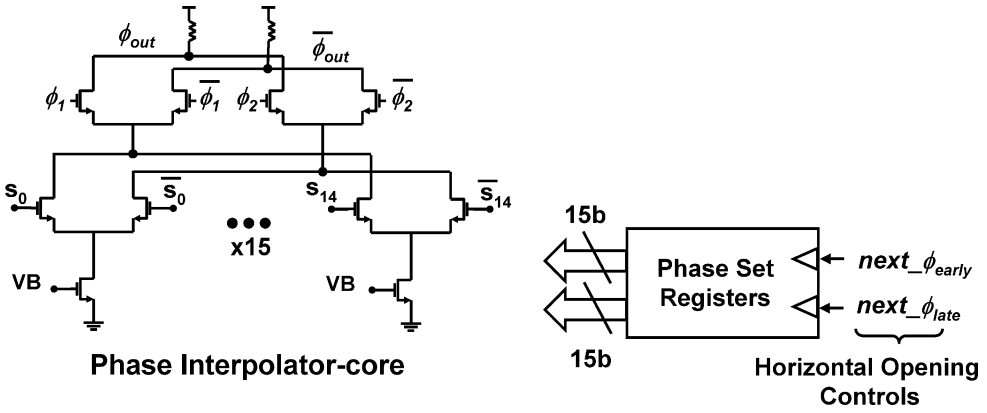

Fig. 9. Phase interpolator and phase-set register.

its sensitivity. The sensitivity of a single-ended comparator is defined as the minimum required amplitude at the input port that makes the output swing to the top rail. The tail current devices are designed longer than the minimum feature size to improve their output impedance and further enhance CMRR. The comparator is optimized to achieve maximum gain bandwidth product. This maximizes the comparators' sensitivity and thus minimizes the degradation of the input eye diagram shape due to EOM nonidealities. We will discuss the impact of EOM nonidealities on the eye opening in Section V.

The comparator's offset is another limitation that affects the EOM operation by shifting the rectangular mask vertically. The input offset for each input source-coupled pair can be modeled by a shift in either V_H or V_L in (2). Equivalently, the overall offset can be modeled as a constant term on the right-hand side of (3). In the absence of offset, comparator maximum sensitivity is when $V_H = V_L$ and both are equal to the input common mode, because then the second term on the right-hand side of (3) is zero. With offset, maximum sensitivity is when $V_H - V_L$ equals the amount of the offset. This interpretation is used to de-embed the offset impact on MER measurements, as will be shown in Section V. In the implementation of the prototype, we minimized offset by careful layout techniques to increase matching between transistors. We also avoided using low-V_t (MOS threshold voltage) devices for the input stage transistors of the comparator due to their poor V_t matching property. Monte Carlo simulation of the comparator shows a mean output offset voltage of 6.4 mV with worst case value of 25 mV. A CML buffer follows the second stage of the comparator to convert the output swing to proper levels for CML DFF blocks in the subsequent stages. DFFs use a standard master–slave topology with conventional CML latches and resistive loads. The clock divider is a static divider based on similar CML latches. We used low-V_t transistors in the latch circuit to enhance the latch switching speed.

The phase rotator circuit consists of a phase interpolator and a phase-set register that adjusts the proper interpolation weight. The phase interpolator is formed by two parallel differential stages, as Fig. 9 shows. The differential input of each stage is connected to one of the two input phases. By properly adjusting the differential control lines s_0–s_{14}, the tail current is steered between the two stages to set the input phase weights and obtain the desired interpolated phase. To generate uniform phase steps and thus uniformly sweep the mask horizontal opening, the transfer characteristic of the phase interpolator, i.e., the relationship between output phase and input weight, should be linear. The characteristic can be controlled by the input signal transition slope and the bandwidth of the interpolator. Fig. 10 illustrates the transfer function for three different bandwidths that is achieved by generalizing the approach in [30]. The phase interpolator is modeled by a band-limited system that performs a weighted sum operation on two input signals. Although a smaller bandwidth linearizes the transfer function, it causes increased jitter because it reduces the output signal transition slope and thus creates more timing uncertainty due to amplitude fluctuation at the signal threshold crossing point.

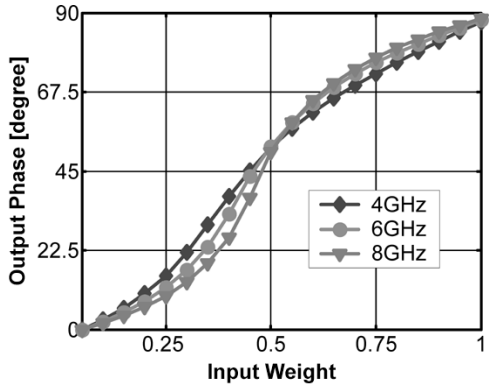

Fig. 10. Simulated phase interpolator transfer function for different bandwidths.

The reference-set register for the DAC, the phase-set registers for the phase rotators, and all the back-end dividers and error combiner are implemented using CMOS standard cells in the technology to achieve lower power consumption.

V. Experimental Results

The EOM circuit was implemented in a 0.13-μm standard CMOS technology. The die photograph and the layout of the active core are shown in Fig. 11. The chip is designed for a customized pad frame that enabled us to perform on wafer testing. As a result, the die size is bounded to the pad frame and is 1.7×1.7 mm^2. However, the active area of the EOM circuit that is highlighted on the die photograph is only 400×660 μm^2. Wafer measurements at up to 12.5 Gb/s input data rate with a

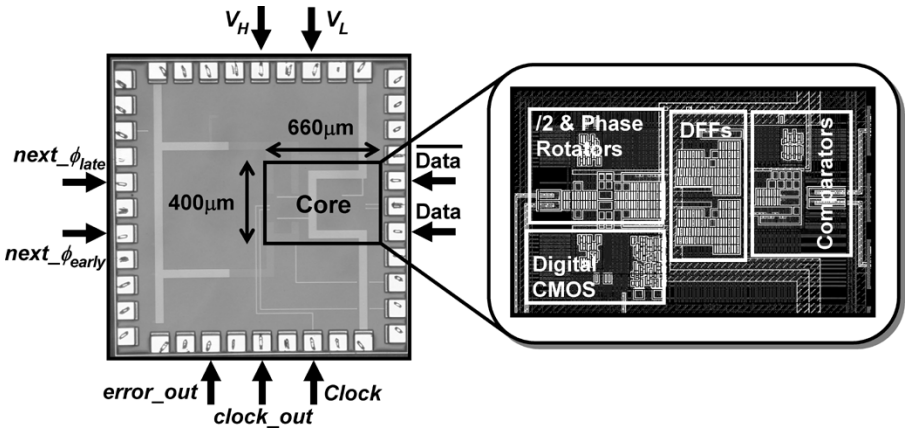

Fig. 11. Die photograph of the EOM with magnified active core.

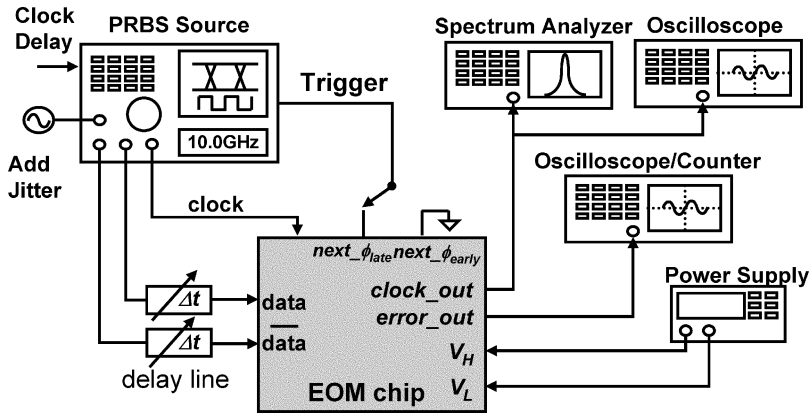

Fig. 12. Measurement setup.

$2^{31}-1$ pseudo-random bit sequence (PRBS) source and 1.2-V power supply showed successful error diagram measurement. Tested input amplitude was from 50 to 400 mVp. The chip consumes about 275 mA from a 1.2-V supply. It is functional at 10 Gb/s with supply voltage as low as 1 V. It operates reliably even at severe input conditions when a closed eye with 10^{-2} BER is applied to the input. In the following, we elaborate on the test setup and experimental results.

A. Test Setup

The block diagram of our test setup is shown in Fig. 12. A PRBS source provides the data and clock for wide range of data rates up to 12.5 Gb/s. The data source has an additional port that controls the amount of jitter added to the data artificially. Although the full rate clock phase is primarily phase-locked to data when applied to the EOM, the on-chip path difference does not preserve the phase relationship. In our measurements, we compensated the path delay mismatch by an external delay line. We adjusted the external delay to minimize the MER for the minimum size mask to guarantee that the mask is centered with respect to the eye. In the adaptive equalizer loop, this calibration can be done once at start up, as the delay mismatch is a systematic effect. In addition, two external delay lines were used at the input path to compensate external cable mismatches and insure 180° phase difference between differential inputs.

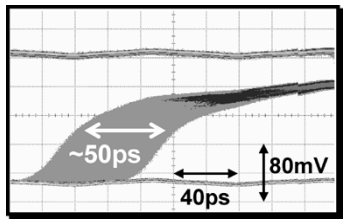

Fig. 13. Accumulated phase of the clock_out signal that verifies the functionality of the divider and phase rotator with a 10-GHz input clock.

The trigger signals for next_$\phi_{\rm early}$ and next_$\phi_{\rm late}$ are applied externally to step horizontal opening of the mask. Similarly, vertical opening is controlled by varying V_H and V_L externally. A frequency counter records the average frequency of the error_out signal, from which MER can be calculated using (1).

B. Clock Path

We first tested the functionality of the divider and the phase rotators by observing the clock_out output signal on the oscilloscope. Fig. 13 shows the accumulated phases of the clock_out when a 10-GHz clock is applied to the clock input. We trigger the next_$\phi_{\rm late}$ signal by applying a 3-MHz square wave pulse. Although standard cell CMOS dividers slow down the clock transition, the accumulated phases correctly cover 50 ps, which is equivalent to half of the bit period of a 10-Gb/s signal.

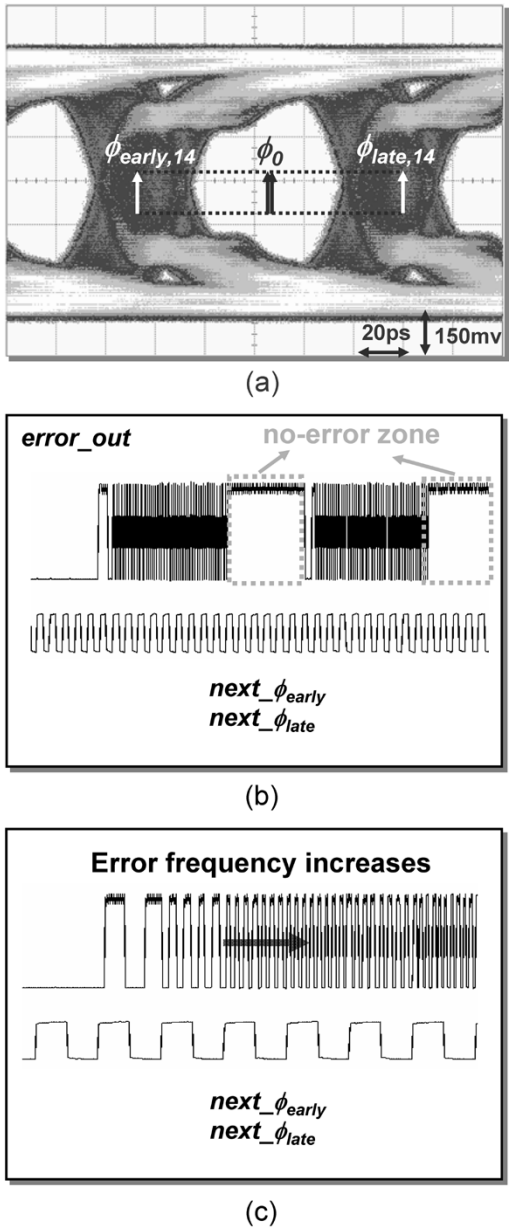

Fig. 14. Qualitative eye-opening measurement. (a) 10-Gb/s input eye diagram. (b) The error_out signal demonstrates an error-free region. (c) Magnified error_out signal shows MER increase for wider mask.

C. Qualitative Eye-Opening Measurement

The objective of this test is to verify the functionality of the main blocks in the data path of the EOM. We apply a 10-Gb/s PRBS input signal and add 41-ps peak-to-peak sinusoidal jitter (SJ) to it to degrade the eye quality, as shown in Fig. 14(a). The next_$\phi_{\rm early}$ and next_$\phi_{\rm late}$ signals are stepped simultaneously. The vertical opening of the mask is constant and is set to 120 mV with external references. Fig. 14(b) shows the measured error_out signal. There is an error-free region (no toggle) for a small mask opening that corresponds to when $\phi_{\rm early}$ and $\phi_{\rm late}$ are close to their initial position in the center of the eye. But as the trigger signals step the sampling phases toward the edges of the eye and thus the mask gets wider, the error frequency gradually increases. This can be seen in Fig. 14(c), which is the magnified error_out signal around regions with error and shows the frequency of error_out signal increases after each positive trigger edge. The periodic behavior of the error_out signal is due to the self-resetting mechanism of the phases.

D. Eye-Opening Measurement Variations

Ultimately, the EOM will be used in an adaptive equalizer as shown in Fig. 1. In such setting, the EOM output should track variations of the eye opening and provide a correct gradient to assist the optimization algorithm in adjusting the filter coefficients. We verified the behavior of the EOM in this scenario by measuring the eye opening when various amounts of peak-to-peak SJ are added to the 10-Gb/s $2^{31}-1$ PRBS input. The vertical opening of the mask is constant. Fig. 15 shows the measurement result with three sample input eye diagrams that demonstrate gradual closing of the eye. As expected, the measured eye opening monotonically decreases as additional jitter closes the eye. At low input jitter, the transition from small to large measured MER is abrupt and thus the plot loses accuracy, because the resolution of horizontal eye-opening step becomes comparable to the peak-to-peak input jitter. Therefore, when the sampling clocks approach the data edge, one horizontal opening step can increase the number of transitions falling inside the mask from zero to all transitions.

E. Complete System Test

This experiment demonstrates the EOM capability in generating the 2-D error diagram that corresponds to the input eye shape. A pair of 5-ft coaxial cables was used to add ISI to the input data. A computer program controls a pulse generator and two external power sources through a general-purpose interface bus (GPIB) port. The program steps through several mask horizontal and vertical openings. A frequency counter records the error_out frequency, as the number of transition errors, for each mask. In each mask sweep, only one half of the eye is covered by triggering only one of the next_$\phi_{\rm early}$ or next_$\phi_{\rm late}$ signals. The other phase is held in the center of the eye in phase with Q. Once one half of the eye is swept completely, the other next signal will be stepped through to cover the other half. This way, any horizontal asymmetry in the eye is captured.

Ideally, when V_H and V_L are both equal to the input data common mode, the MER should be minimum because the comparators have the highest sensitivity. Therefore, the vertical mask is swept for $V_H = V_{\rm cm} + n\Delta V$ and $V_L = V_{\rm cm} - n\Delta V$, where $V_{\rm cm}$ is the data common mode and $1 \le n \le N$. N is 7 if an on-chip DAC is used but can be larger with external reference adjustment. However, due to comparators' offset, the minimum error count may occur when $V_H \le V_{\rm cm}$ or $V_L \ge V_{\rm cm}$. To guarantee that all the horizontal range is covered, the horizontal sweep is done for $-N \le n \le N$. We measured a total of three samples and we observed that the minimum MER occurs at $n = 1$ or 2 corresponding to 5–10 mV of differential offset for the three samples.

Fig. 16 illustrates the 2-D error diagram that is generated as the result of the measurement for the input eye in Fig. 14(a). It demonstrates that the asymmetrical input eye shape is captured. Furthermore, the diagram has 68 dB of dynamic range for MER. The dynamic range is a function of the time period for MER

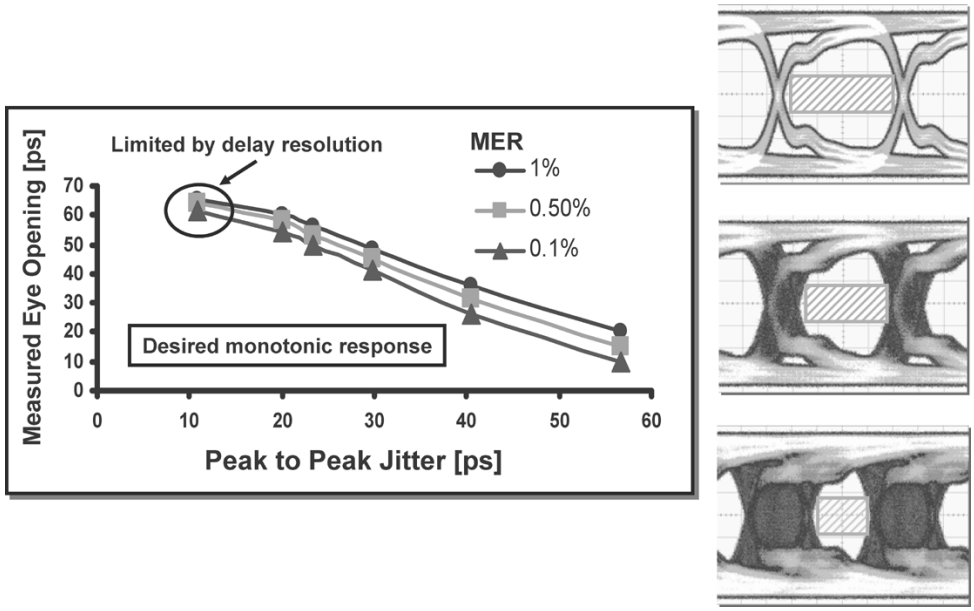

Fig. 15. Measured eye opening for various input eye diagrams with different peak-to-peak jitter.

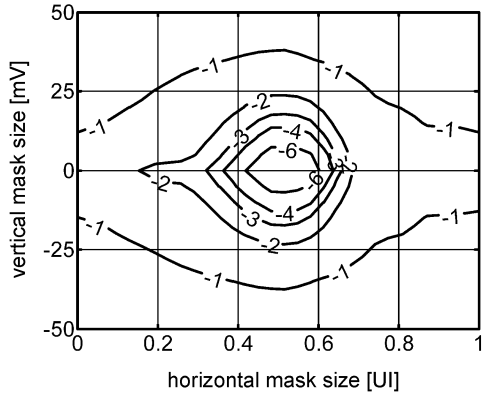

Fig. 16. Measured 2-D error map with 68-dB dynamic range.

measurement per one mask. A longer period of error-free measurement corresponds to a smaller MER.

We show in the Appendix that the MER measured by an ideal EOM can be expressed as

$$\text{MER} \cong Q\left(\frac{1-(V_H-V_L)}{2\sigma}\right) \tag{4}$$

for a signal amplitude of "1" and input noise standard deviation of σ. Amplitude noise is assumed to have Gaussian distribution and $Q(.)$ is its cumulative distribution function. Due to the exponential nature of $Q(.)$, the expected MER is about four orders of magnitude larger than BER for a BER of about 10^{-12}.

The nonidealities of the EOM, specifically the bandwidth limitations of the comparators, further degrade the measured MER. It is shown in the Appendix that (4) can be modified to

$$\text{MER} \cong Q\left(\frac{A(t)-(V_H-V_L)}{2\sigma}\right) \times\left(1-Q\left(\frac{A(t)+(V_H-V_L)}{2\sigma}\right)\right) \tag{5}$$

to take the impact of the EOM into account. $A(t)$ is the response of the comparator to the input sequence at the time of sampling t. As the sampling clocks, ϕ_{early} or ϕ_{late} is stepped toward the edges of the eye diagram, $A(t)$ approaches the threshold level, and MER increases as a consequence. A 2-D MER map can be obtained from (5) for different sampling times and $V_H - V_L$ based on the input and comparator response. We generated this error map using the simulation results of the comparator in our design and compared it with the measured 2-D error map in Fig. 16. A 2-D cross-correlation of the two maps resulted in a 0.9 correlation coefficient that verifies our measurement is closely following the expected result from simulation.

F. EOM Versus BERT

The EOM has two main features that distinguish it from a conventional BER test (BERT) system. First, the EOM detects errors based on two samples at the same sampling phase. It does not require pattern matching. Thus, unlike a BERT that requires a PRBS sequence for proper operation, the EOM can operate with truly random sequences and does not need the *a priori* knowledge of the transmitted sequence. This simplifies the error detection computation and hardware remarkably. Second, a BERT treats the channel's deterministic impacts, amplitude noise, random jitter, and digital errors induced from the imperfect digital circuit blocks, e.g., multiplexer and demultiplexer, equally. Therefore, the effect of the individual impairments on the number of detected errors cannot be separated. However, the digital errors are ignored by the EOM as it does not compare received data with a predetermined sequence. For instance, if a data "1" is converted to data "0" due to multiplexer noise and then sent over the channel, the EOM operation will not be affected, whereas the BERT will count an error. Consequently, the error count is mainly correlated to the impact of the channel response. Fig. 17 compares the response of the EOM and a commercial BERT in the presence of digital errors intentionally added to the input. A 12.5-Gb/s $2^{31}-1$

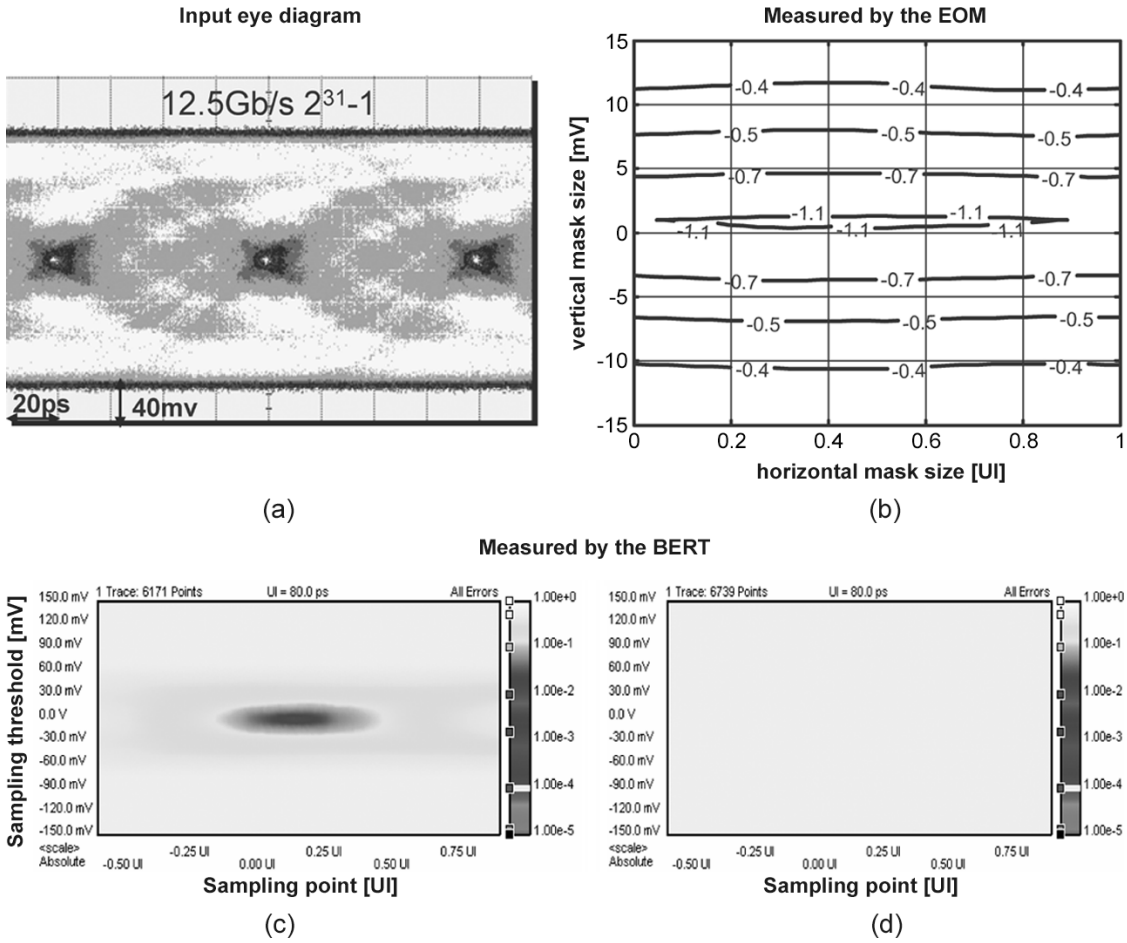

Fig. 17. Comparing EOM and BERT operations. (a) 12.5-Gb/s input eye. (b) MER measurement with EOM in the presence of 10% digital error. (c) BER measured with commercial BERT. (d) BER measured with commercial BERT in the presence of 10% digital error.

PRBS is passed through 5 ft of lossy coaxial cable to introduce ISI and is then applied to the input of the EOM or BERT. The eye diagram is closed and is shown in Fig. 17(a). Fig. 17(c) is the response of the BERT with about 18-dB BER dynamic range. However, when 10% digital error is added to the input, the BERT cannot capture the eye diagram shape although the channel has not changed. Evidently, from Fig. 17(d), the BERT has lost its error dynamic range completely. Fig. 17(b) is the response of the EOM in the presence of digital errors and demonstrates that EOM successfully captures the shape of the eye diagram as in Fig. 17(b). The MER dynamic range is reduced to about 8 dB due to the reasons discussed in Section V-E.

VI. Conclusion

An architecture that can essentially capture a 2-D map of the eye diagram of a high-speed data signal has been developed. The error map can be used to extract various features of the received signal. Specifically, it can be used in an adaptive equalizer to generate the signal quality as the cost function for coefficient optimization. The cost function will solely depend on the quality of the received signal and not on the decision of the receiver.

The architecture is based on comparing two samples of the signal at one sampling point and therefore does not require *a priori* knowledge of data sequence or pattern matching that remarkably simplifies the architecture. A prototype was implemented in 0.13-μm standard CMOS technology that was successfully tested up to 12.5 Gb/s input data rate. It consumes about 275 mA from a 1.2-V supply, which is significantly lower than prior art.

Appendix

We assume the amplitude noise cumulative distribution function is $Q()$. The probability of a mask error occurring is

$$\text{MER} = \Pr\{S_H \neq S_L\} \tag{6}$$

where $\Pr\{\}$ denotes the probability and S_H and S_L are defined in Section II. S_H and S_L take binary values and thus there are two combinations that contribute to (6). The probability of each of the combinations can be calculated conditioned on the input bit to the EOM. Therefore, we have

$$\begin{aligned}\text{MER} = \frac{1}{2}\,(&\Pr\{S_H = 0\; S_L = 1 | \text{in} = 1 + z\} \\ &+ \Pr\{S_H = 0\; S_L = 1 | \text{in} = z\} \\ &+ \Pr\{S_H = 1\; S_L = 0 | \text{in} = z\} \\ &+ \Pr\{S_H = 1\; S_L = 0 | \text{in} = 1 + z\})\end{aligned} \tag{7}$$

where z is the input noise at sampling point. When the EOM is ideal, only input noise impacts S_H and S_L values. The last two

terms in (7) will be identically zero because they both imply $V_H < V_L$. The first two terms both equal the probability that

$$\frac{1-(V_H-V_L)}{2} < z < \frac{1+(V_H-V_L)}{2}. \tag{8}$$

Hence, we can write

$$\begin{aligned}\text{MER} &= Q\left(\frac{1-(V_H-V_L)}{2\sigma}\right) - Q\left(\frac{1+(V_H-V_L)}{2\sigma}\right)\\ &\cong Q\left(\frac{1-(V_H-V_L)}{2\sigma}\right).\end{aligned} \tag{9}$$

The approximation holds when $V_H \gg V_L$. When the impact of ISI introduced by the EOM is considered, the last two terms in (7) are not identical to zero anymore because S_H and S_L are the output of two comparators with different noise contribution. However, we can still neglect them in MER calculation for reasonable noise levels in the comparators. The first term in (7) can be written as

$$\begin{aligned}&\Pr\{S_H = 0\, S_L = 1 | \text{in} = 1+z\}\\ &\quad = \Pr\{S_H = 0 | \text{in} = 1+z\} \cdot \Pr\{S_L = 1 | \text{in} = 1+z\}.\end{aligned} \tag{10}$$

Because of the bandwidth limitations of the comparators, the probabilities on the right side of (10) are functions of the sampling time and are smaller when the sampling time is closer to the data edge. If the response of the comparators to the input is denoted by $y(t)$, we have

$$y(t) = \sum_i A_i(t). \tag{11}$$

We define $A_i(t)$ as the response of the comparators to the input in a unit interval $(i-1)T < t < iT$, where T is the bit period. Several $A_i(t)$ exist due to the various combination of symbols that cause ISI. The overlap of $A_i(t)$ for all i when transformed to $0 < t < T$ is the eye diagram. If we limit ISI to the last n symbols, only 2^n distinct $A_i(t)$ could be achieved for a binary modulation. Then, from (10), we can write

$$\begin{aligned}\text{MER} \cong \frac{1}{2^n}\sum_{i=1}^{2^n} &Q\left(\frac{A_i(t)-(V_H-V_L)}{2\sigma}\right)\\ &\times\left(1-Q\left(\frac{A_i(t)+(V_H-V_L)}{2\sigma}\right)\right).\end{aligned} \tag{12}$$

For simplicity, we rewrite (12) as

$$\begin{aligned}\text{MER} \cong Q&\left(\frac{A(t)-(V_H-V_L)}{2\sigma}\right)\\ &\times\left(1-Q\left(\frac{A(t)+(V_H-V_L)}{2\sigma}\right)\right)\end{aligned} \tag{13}$$

where the sum is implicit in the notation. Equation (12) can be used to generate a 2-D map of the MER, which is the expected result from the measurement for a given input eye diagram. We verified that our measurement result is very closely correlated to it.

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